


**FIG. 1**


200 

SILICON LAYER  
230

BURIED OXIDE  
220

Si SUBSTRATE  
210

**FIG. 2**

200 

N-CHANNEL

P-CHANNEL

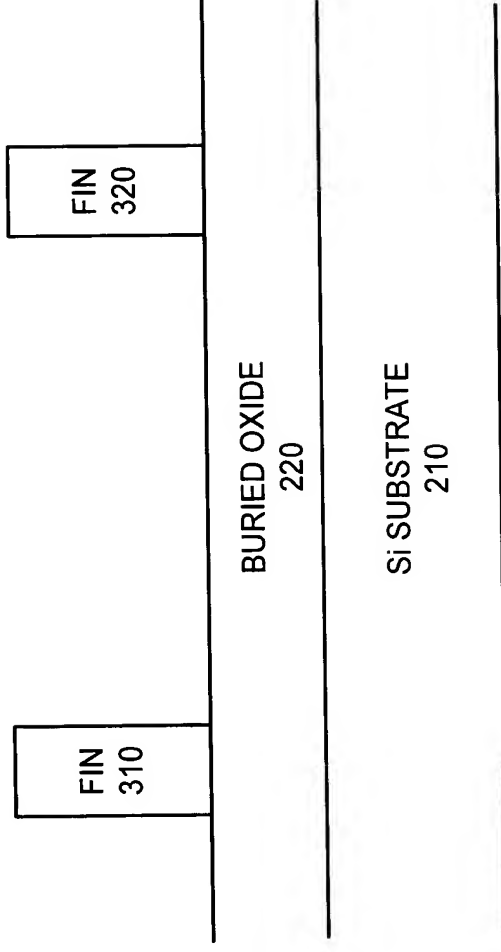


FIG. 3A

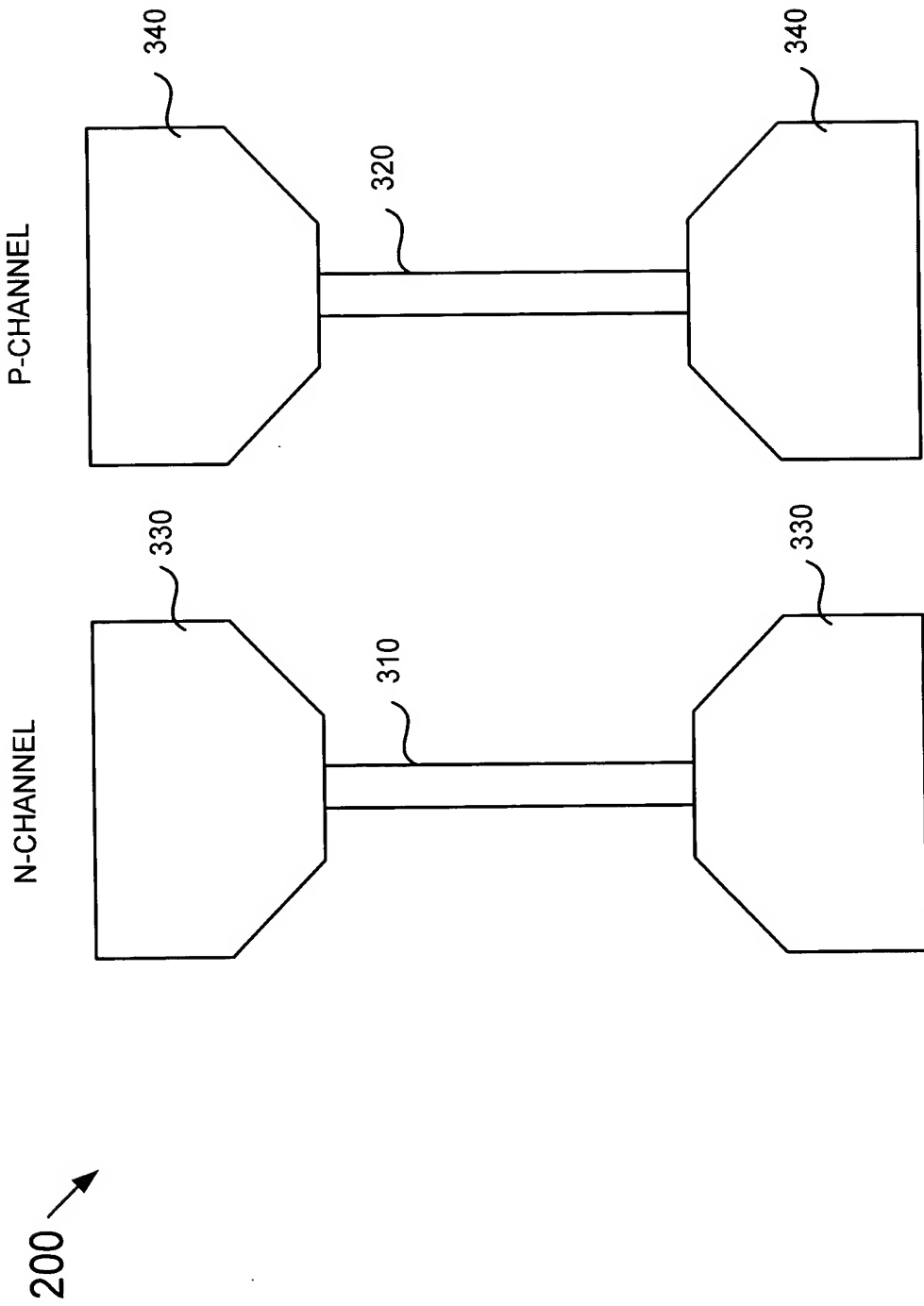


FIG. 3B

200 →

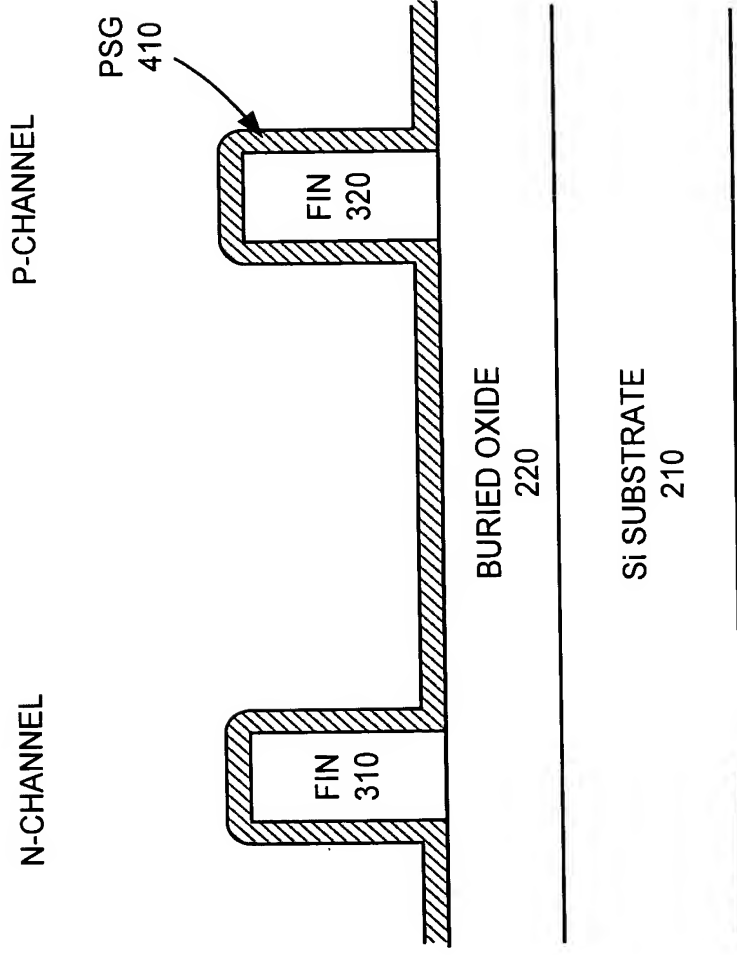


FIG. 4

200

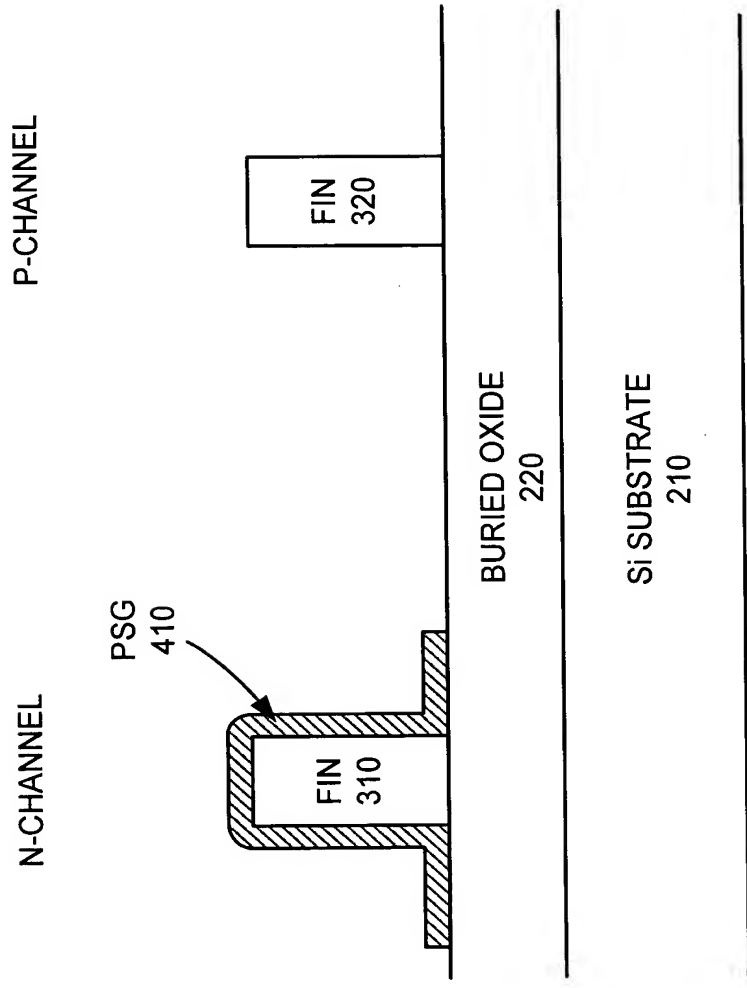


FIG. 5

200 →

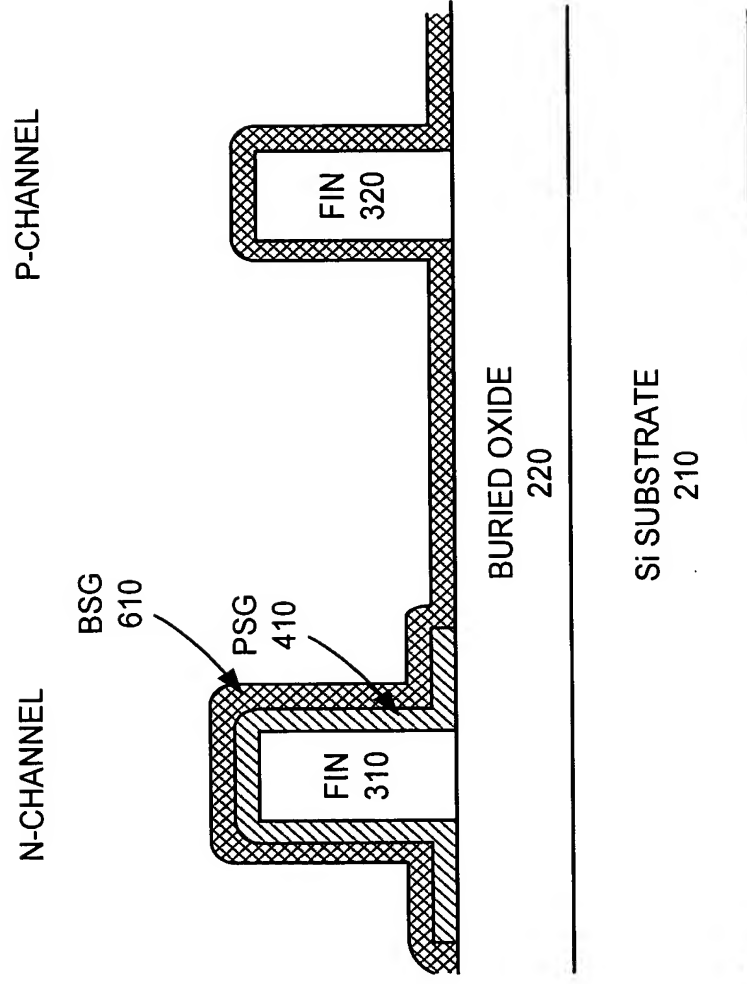


FIG. 6

200

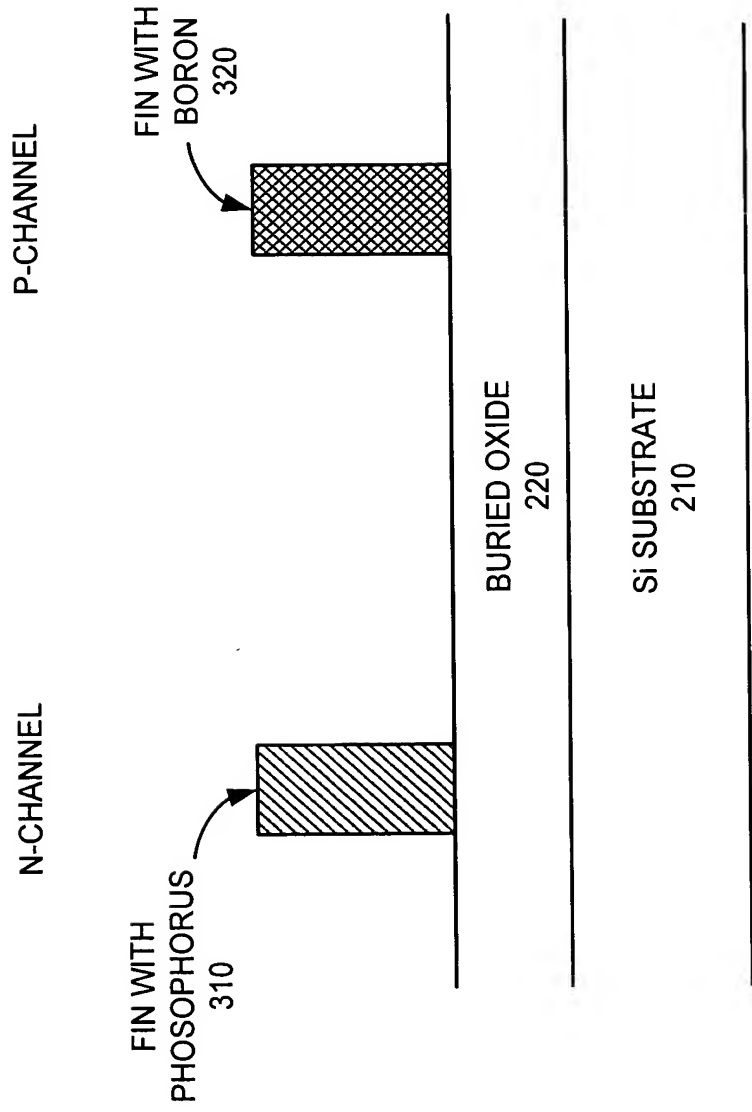


FIG. 7A



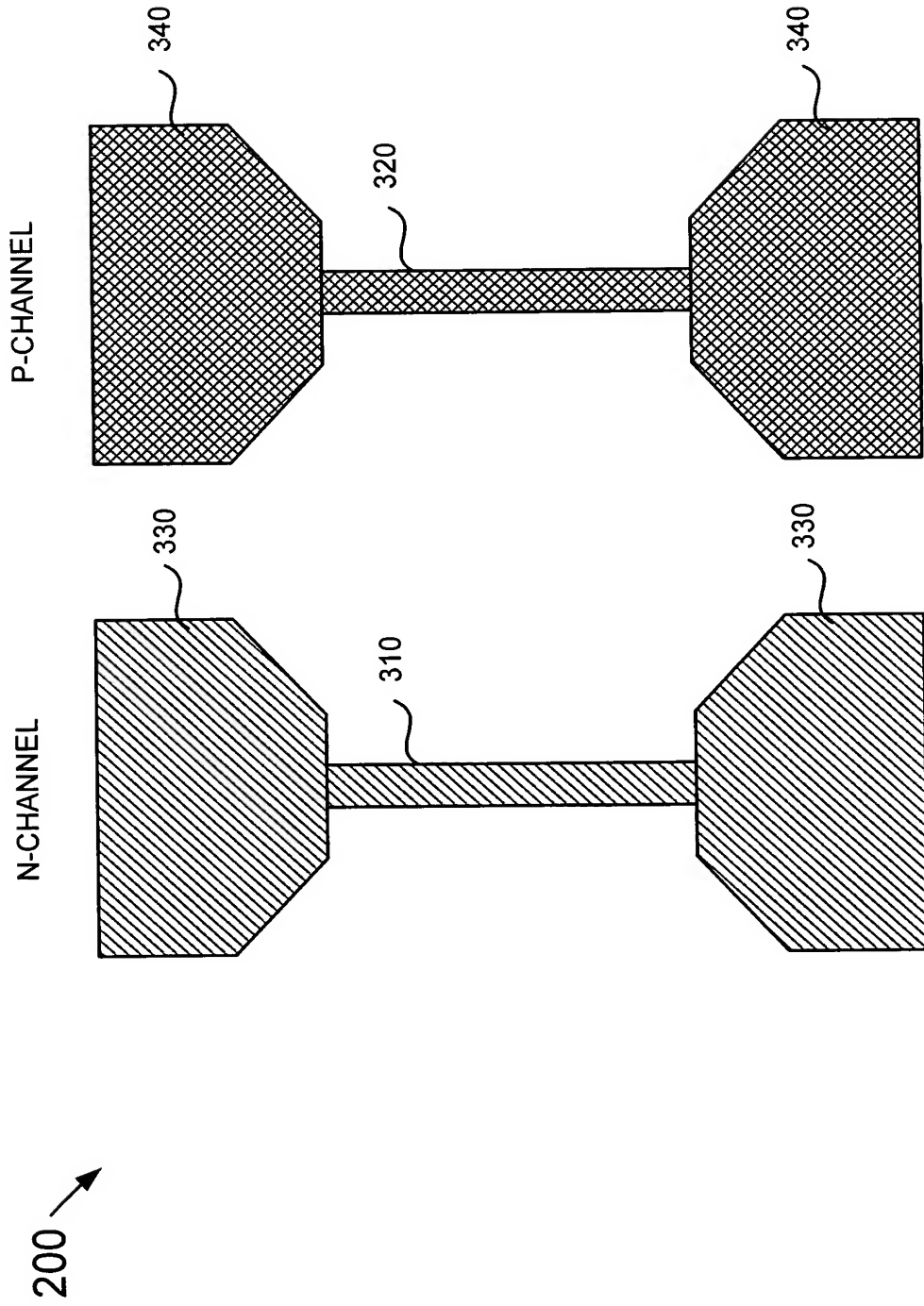


FIG. 7B

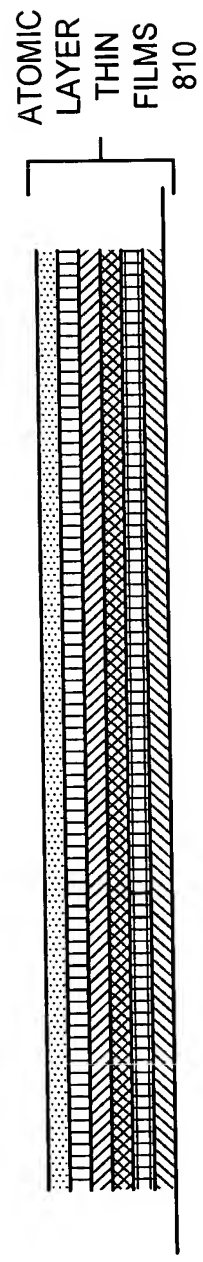


FIG. 8